



MosChip Security Processor MCS1000

Data Brief

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General Description

The MosChip Security Processor™ (MCS1000) is a highly integrated VPN System-On-a-Chip with three 10/100 Ethernet interfaces. The MCS1000 can run in peripheral mode and act as a secure Fast Ethernet controller or it can operate in standalone mode and perform all VPN, firewall, and gateway functions independently. The MCS1000 consists of three function groups: a CPU Subsystem, VPNow™ Hardware Module, and General Interface Blocks. The CPU Subsystem contains an ARM926EJ-S, 200MHz, 32-bit RISC microprocessor delivering approximately 1.1 MIPS per MHz. The core processor handles all housekeeping functions on the MCS1000 and it is tightly integrated to the VPNow™ Hardware Module (cryptographic co-processor). The VPNow™ Hardware Module handles all IPsec functions. It has been designed around the IPsec specification and implements DES, 3DES, AES, MD5, and SHA-1 and SHA-256 algorithms. The maximum bandwidth through the VPNow™ Hardware Module is 400Mbps. The VPNow™ HW module executes built-in microcode and the CPU fetches code only from SDRAM. The General Interface Blocks consists of a Memory Controller, PCI Controller, Ethernet interface, and General I/O interface.

The Memory Controller can interface to standard SDRAM and Flash or any standard non-volatile memory. The SDRAM controller supports up to 64 Mega bits of SDRAM through a 32-bit bus. The non-volatile memory controller can interface to 8-, 16- or 32-bit wide devices and has 26 address lines for up to $2^{26} = 64$ Mega Bytes of storage per chip select. The Memory Controller has a local bus interface that supports 8-, 16- and 32-bit devices. This high-bandwidth bus can be used for additional peripheral expansion such as USB or 1394 interfaces. The Peripheral bus has a programmable ready signal and an interrupt input. The waveforms for all control signals are programmable in bit-mapped waveform registers. The PCI interface is a 32-bit 33MHz interface and it complies with the PCI 2.2 standard. The internal PCI controller can be a slave device and can master the bus, but it does not contain a PCI arbiter and does not have a internal memory window for external master burst access. . The PCI interface can also function as a CardBus interface for use in PCMCIA applications.

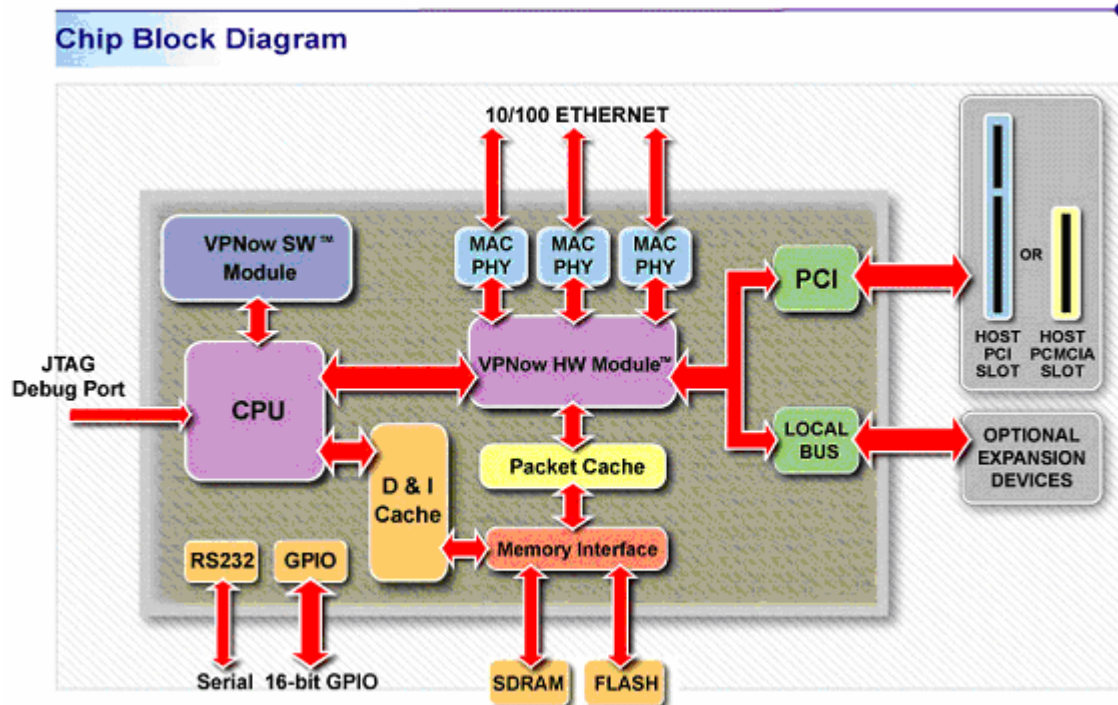
There are three (3) 10/100 Ethernet controllers integrated into the MCS1000. Each controller consists of an independent Media Access Controller (MAC) and Physical layer (PHY). The Ethernet interfaces can be connected directly to external magnetics, LEDs and connectors. Ethernet A can also be connected to an optical interface.

The MCS1000 has an alternate Ethernet configuration. In this configuration the third Ethernet interface (Ethernet C) does not use the internal PHY and its MII is available on the external pins. In this configuration LED signals for Ethernet A and B, eight (8) GPIO and three (3) UART control signals are all lost. This configuration is controlled via pull-ups and pull-downs on the four (4) configuration pins and cannot be entered through software.

The General I/O interface has 16 bits of GPIO, a serial port and a JTAG interface. The GPIO is controlled by the core processor and can be used for any general bit manipulation and control. The serial interface is a standard RS-232 port (requires external RS-232 level drivers) and is available for user implementation through OS drivers. The JTAG port is reserved for test and debug only. It is possible to connect to ARM core through this port and debug the execution through sideband bus.

There are many applications in which the MCS1000 can enhance performance and security. It can perform all IPsec functionality and offload a host processor of the math intensive IPsec cryptographic processing. It can add encryption to any Ethernet-based system that would benefit from added security and requires no degradation of system performance. It also can be a low-cost high performance VPN/firewall System-On-a-Chip. See MosChip Security Processor™ VPN Application Note.

Figure. Block Diagram



MCS1000 Feature List

- ARM926EJ-S, 32-bit RISC core @ 200MHz
- 32KB instruction cache / 32KB data cache
- 32KB internal boot ROM
- Operates in standalone or peripheral modes_
- Three 10/100Mbps Ethernet cores in full-duplex mode (up to 400Mbps)
- 32-bit, 33MHz PCI with PCMCIA (CardBus) support
- 100MHz SDRAM interface
- 16-bit GPIO
- Serial Port interface for debug terminal
- JTAG interface for boundary-scan/debug and test
- Hardware cryptography block that supports:
 - Lookup unit for search acceleration
 - 16KB VPNow™ packet cache
 - Standards: SHA, MD5, DES, 3DES, and AES
 - Real-time encryption and decryption
 - Transport and tunnel modes supported

Theory of Operation

The MCS1000 has two modes of operation: standalone and peripheral modes. In standalone mode the MCS1000 operates as an autonomous device. This configuration is ideal for low-cost VPN/Firewall boxes. In peripheral mode the MCS1000 interfaces with a host processor via the PCI bus. In this configuration the MCS1000 would function as a secure Ethernet interface chip.

Power-up

The MCS1000 polls its Bootstrap pins upon the reset pin going inactive. The bootstraps set-up clocking and other attributes, described later in the document. The MCS1000 then executes the code in its internal VPNow™ Software Module in order to set-up the ARM processor and the VPNow™ Hardware Module. The MCS1000 will then attempt to fetch instructions from the external Flash. If the MCS1000 is unable to fetch instructions from the flash, then it will wait in an idle mode until the code is downloaded from the PCI bus host.

Standalone Mode

In standalone mode the MCS1000 operates autonomously and does not require a host to supervise the operation of the MCS1000. The internal ARM processor fetches instructions from the external Flash. In this mode the PCI bus is inactive.

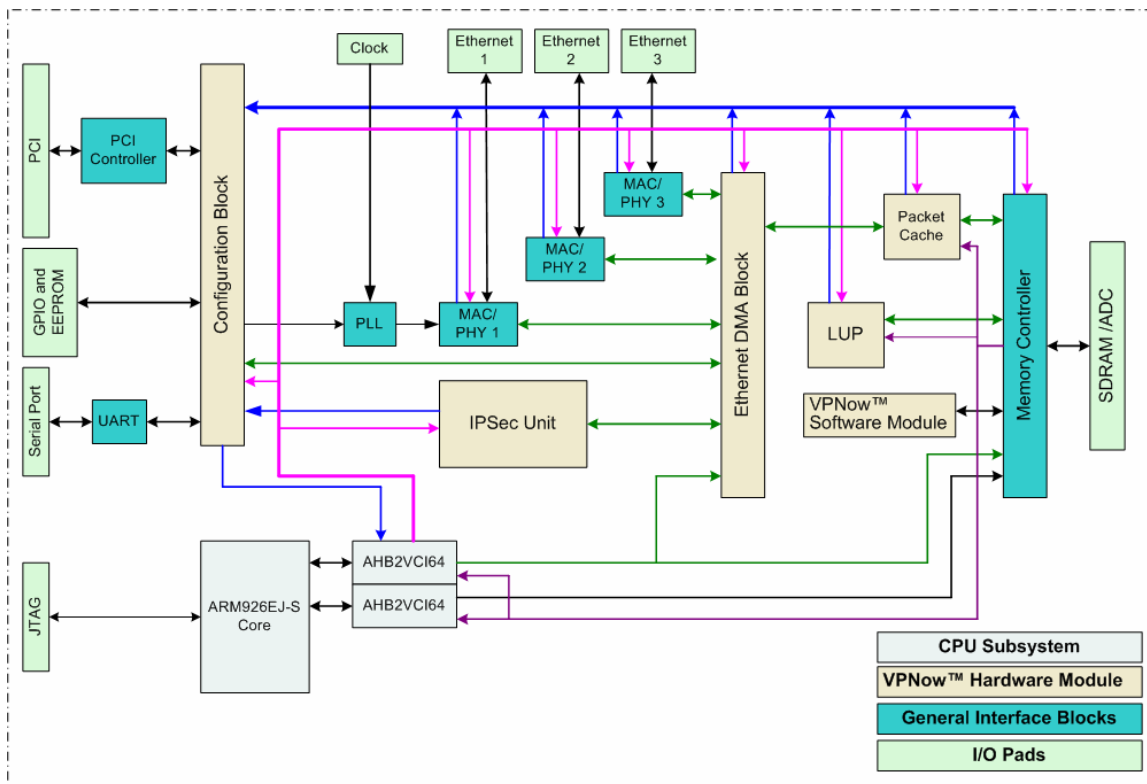
Peripheral Mode

In peripheral mode the MCS1000 functions as a secure Fast Ethernet controller. The MCS1000 is a device on a PCI bus. The control log is stored at the host level, but the Security Policy Database (SPD) and the Security Association Database (SAD) is stored in the MCS1000's local memory. The control log and Internet Key Exchange are left to the host processor.

Internal Architecture

The MCS1000 consists of a CPU Subsystem, VPNow™ Hardware Module and General Interface Blocks. See Figure. Internal Architecture below. The CPU subsystem consists of the ARM926EJ-S core and two (2) AHB to VCI bridges. The MCS1000 contains IPsec specific hardware for accelerating the IPsec protocol known as the VPNow™ Hardware Module. The VPNow™ Hardware Module consists of an IPsec Unit that contains the DES, 3DES and AES cryptography blocks and the MD5 and SHA authentication blocks, 16K Packet Cache, look-up accelerator (LUP), Ethernet DMA Block, Configuration Block and the VPNow™ Software Module. There are also interface blocks known as General Interface Blocks. The General Interface Blocks consist of three (3) Ethernet controllers, PCI interface, Memory Controller (SDRAM, Flash and Local-bus), serial port, General Purpose Input and Output (GPIO) interface, and PLL Cloning Circuit.

Figure. Internal Architecture



Description of Blocks:

CPU Subsystem

- ARM926EJ-S – ARM9 32-bit RISC CPU
- AHB2VCI64 - AHB 32-bit bus to VCI 64-bit bus (2)

VPNow™ Hardware Module

- Configuration Block** - configuration registers and miscellaneous system interfaces
- Ethernet DMA Block** - DMA channels and access arbiter for MAC, PCI and Cipher Module
- LUP**- Table lookup engine for search acceleration
- Packet Cache** – Ethernet packet cache (write-back, write-allocate) with large line size (16 double words)
- IPSec Unit** - Contains the DES, 3DES, and AES cryptographic blocks; MD5 and SHA authentication blocks; and I/O blocks.
- VPNow™ Software Module** – Internal ROM with BIST and initialization code

General Interface Blocks

- PCI Controller** – 32-bit 33MHz PCI 2.2 interface (device only)
- UART** – Standard serial port with LVCMOS logic level input/output
- PLL** – Phase Locked Loop used to generate internal clocks.
- MAC/PHY**- Ethernet interface to external magnetics
- Memory Controller** - Memory controller back-end for flash and SDRAM, arbiter mux between CPU, LUP and packet cache

Pin List by Group

Table. General Purpose I/O (GPIO) Pin List

GPIO Pin List				
Pin Name	Location	I/O/P	Type	Description
GPIO[0]	M17	I/O	J	General Purpose IO line 0
GPIO[1]	N20	I/O	J	General Purpose IO line 1
GPIO[2]	N19	I/O	J	General Purpose IO line 2
GPIO[3]	N18	I/O	J	General Purpose IO line 3
GPIO[4]	P20	I/O	J	General Purpose IO line 4
GPIO[5]	P19	I/O	J	General Purpose IO line 5
GPIO[6]	R20	I/O	J	General Purpose IO line 6
GPIO[7]	R19	I/O	J	General Purpose IO line 7
GPIO[8]	P17	I/O	J	General Purpose IO line 8
GPIO[9]	R18	I/O	J	General Purpose IO line 9
GPIO[10]	T20	I/O	J	General Purpose IO line 10
GPIO[11]	T19	I/O	J	General Purpose IO line 11
GPIO[12]	T18	I/O	J	General Purpose IO line 12
GPIO[13]	U20	I/O	J	General Purpose IO line 13
GPIO[14]	V20	I/O	J	General Purpose IO line 14
GPIO[15]	T17	I/O	J	General Purpose IO line 15

Table. JTAG and Reset Interface

JTAG and Reset Interface				
Pin Name	Location	I/O/P	Type	Description
POR_N	M19	I	L	System Reset. Minimum duration is 10 mS.
RST_OUT_N	M18	O	B	Reset out for other components on board. Same as System Reset re-driven. Delay from POR_N is <1 ns.
TCK	V4	I	L	JTAG chain clock
TDI	W4	I	L	JTAG chain input
TDO	Y2	O	D	JTAG chain output
TMS	U5	I	L	JTAG chain TMS

Table. Serial EEPROM Interface

Serial EEPROM Interface				
Pin Name	Location	I/O/P	Type	Description
EEPIO[0]	R2	I/O	E	EEPROM I/O, programmable, SK
EEPIO[1]	T1	I/O	E	EEPROM I/O, programmable, SI
EEPIO[2]	P4	I/O	E	EEPROM I/O, programmable, SO
EEPIO[3]	R3	I/O	E	EEPROM I/O, programmable, CS#

Table. Serial Port Interface

Serial Port Interface				
Pin Name	Location	I/O/P	Type	Description
CTS_N	W1	I	L	Clear To Send. A control signal to the MCS1000. The remote device is ready to receive input.
DCD_N	W3	I	L	Data Carrier Detect
DSR_N	W2	I	L	Data Set Ready. A control signal to the MCS1000. The modem is ready to answer or originate a call.
DTR_N	Y1	O	B	Data Terminal Ready. A control signal from the MCS1000. The MCS1000 uses this to enable the modem: the modem is allowed to go on-line or answer a call.
RI_N	U3	I	L	Ring Indicator.
RTS_N	V3	O	B	Request To Send. A control signal from the MCS1000. The MCS1000 is ready to receive data.
RXD	T4	I	L	Receive data line.
TXD	T2	O	B	Transmit data line.

Table. PHY Interface

PHY Interface				
Pin Name	Location	I/O/P	Type	Description
ETH_A_5K	M3	I	A	Band-gap reference voltage, must be tied to ground with 5K +/- 1% resistor.
ETH_A_LED[0]	A2	O	C	Ethernet A LED TX/RX
ETH_A_LED[1]	B2	O	C	Ethernet A LED LINK 100
ETH_A_LED[2]	B3	O	C	Ethernet A LED LINK 10
ETH_A_RXN	F1	I	O	10/100 receive data channel A Negative (-).
ETH_A_RXP	F2	I	O	10/100 receive data channel A Positive (+).
ETH_A_SDN	B1	I	A	Signal Detect Negative - FX mode only
ETH_A_SDP	E4	I	A	Signal Detect Positive - FX mode only
ETH_A_TXN	E1	O	N	10/100 transmit data channel A Negative (-)
ETH_A_TXP	E2	O	N	10/100 transmit data channel A Positive (+)
ETH_B_LED[0]	G2	O	C	Ethernet B LED TX/RX
ETH_B_LED[1]	G1	O	C	Ethernet B LED LINK 100
ETH_B_LED[2]	H3	O	C	Ethernet B LED LINK 10
ETH_B_RXN	L2	I	O	10/100 receive data channel B Negative (-).
ETH_B_RXP	L1	I	O	10/100 receive data channel B Positive (+).
ETH_B_TXN	K2	O	N	10/100 transmit data channel B Negative (-)
ETH_B_TXP	J1	O	N	10/100 transmit data channel B Positive (+)
ETH_C_LED[0]	J3	O	I	Ethernet C LED TX/RX
ETH_C_LED[1]	J4	O	I	Ethernet C LED LINK 100
ETH_C_LED[2]	H1	O	I	Ethernet C LED LINK 10
ETH_C_RXN	N2	I	O	10/100 receive data channel C Negative (-).
ETH_C_RXP	N3	I	O	10/100 receive data channel C Positive (+).
ETH_C_TXN	R1	O	N	10/100 transmit data channel C Negative (-)
ETH_C_TXP	P3	O	N	10/100 transmit data channel C Positive (+)

Table. Clock Interface

Clock Interface				
Pin Name	Location	I/O/P	Type	Description
ETH_X1	M4	I	A	25MHz oscillator input/crystal input. If a clock oscillator is used, then this pin is used.
ETH_X2	N1	O	A	25MHz crystal input. If a clock oscillator is used, then this pin is left unconnected.

Table. Memory Controller: SDRAM, Flash and Local-bus Interface

Memory Controller: SDRAM, Flash and Local				
Pin Name	Location	I/O/P	Type	Description
ADC CLK	L19	O	B	Local Bus Clock
ADC CS N[0]	J18	O	B	Local Bus chip select 0, Active low.
ADC CS N[1]	J19	O	B	Local Bus chip select 1, Active low.
ADC CS N[2]	J20	O	B	Local Bus chip select 2, Active low.
ADC CS N[3]	K19	O	B	Local Bus chip select 3, Active low.
ADC RD N	L20	O	B	Local Bus Read
ADC RDY	L18	I	L	Local Bus I/O Ready
ADC WR N	K20	O	B	Local Bus Write, Active low
SDRAM ADDR[0]	A18	O	C	Address bit 0 for SDRAM interface and Local Bus
SDRAM ADDR[1]	E20	O	C	Address bit 1 for SDRAM interface and Local Bus
SDRAM ADDR[2]	G17	O	C	Address bit 2 for SDRAM interface and Local Bus
SDRAM ADDR[3]	D20	O	C	Address bit 3 for SDRAM interface and Local Bus
SDRAM ADDR[4]	E18	O	C	Address bit 4 for SDRAM interface and Local Bus
SDRAM ADDR[5]	E19	O	C	Address bit 5 for SDRAM interface and Local Bus
SDRAM ADDR[6]	D19	O	C	Address bit 6 for SDRAM interface and Local Bus
SDRAM ADDR[7]	C20	O	C	Address bit 7 for SDRAM interface and Local Bus
SDRAM ADDR[8]	D18	O	C	Address bit 8 for SDRAM interface and Local Bus
SDRAM ADDR[9]	C19	O	C	Address bit 9 for SDRAM interface and Local Bus
SDRAM ADDR[10]	B18	O	C	Address bit 10 for SDRAM interface and Local Bus
SDRAM ADDR[11]	C18	O	C	Address bit 11 for SDRAM interface and Local Bus
SDRAM ADDR[12]	C17	O	C	Address bit 12 for SDRAM interface and Local Bus
SDRAM ADDR[13]	D16	O	C	Address bit 13 for SDRAM interface and Local Bus
SDRAM ADDR[14]	B17	O	C	Address bit 14 for SDRAM interface and Local Bus
SDRAM ADDR[15]	F18	O	C	Address bit 15 for SDRAM interface and Local Bus
SDRAM ADDR[16]	E17	O	C	Address bit 16 for SDRAM interface and Local Bus
SDRAM ADDR[17]	B20	O	C	Address bit 24 for SDRAM interface and Local Bus
SDRAM ADDR[18]	F19	O	H	Address bit 18 for SDRAM interface and Local Bus
SDRAM ADDR[19]	G18	O	H	Address bit 19 for SDRAM interface and Local Bus
SDRAM ADDR[20]	G19	O	H	Address bit 20 for SDRAM interface and Local Bus
SDRAM ADDR[21]	G20	O	H	Address bit 21 for SDRAM interface and Local Bus
SDRAM ADDR[22]	H18	O	H	Address bit 22 for SDRAM interface and Local Bus
SDRAM ADDR[23]	H19	O	H	Address bit 23 for SDRAM interface and Local Bus
SDRAM ADDR[24]	H20	O	H	Address bit 24 for SDRAM interface and Local Bus
SDRAM ADDR[25]	J17	O	H	Address bit 25 for SDRAM interface and Local Bus
SDRAM CAS N	B15	O	B	CAS for SDRAM interface
SDRAM CK	A14	O	B	SDRAM clock
SDRAM CS N[0]	A16	O	B	Device select signal 0 for SDRAM memory chips
SDRAM CS N[1]	B16	O	B	Device select signal 1 for SDRAM memory chips
SDRAM CS N[2]	A17	O	B	Device select signal 2 for SDRAM memory chips
SDRAM CS N[3]	C16	O	B	Device select signal 3 for SDRAM memory chips
SDRAM DATA[0]	C4	I/O	K	Data bit 0 for SDRAM interface and Local Bus.
SDRAM DATA[1]	D5	I/O	K	Data bit 1 for SDRAM interface and Local Bus.
SDRAM DATA[2]	A3	I/O	K	Data bit 2 for SDRAM interface and Local Bus.
SDRAM DATA[3]	C6	I/O	K	Data bit 3 for SDRAM interface and Local Bus.
SDRAM DATA[4]	C7	I/O	K	Data bit 4 for SDRAM interface and Local Bus.
SDRAM DATA[5]	B6	I/O	K	Data bit 5 for SDRAM interface and Local Bus.

Memory Controller: SDRAM, Flash and Local				
Pin Name	Location	I/O/P	Type	Description
SDRAM_DATA[6]	A6	I/O	K	Data bit 6 for SDRAM interface and Local Bus.
SDRAM_DATA[7]	C8	I/O	K	Data bit 7 for SDRAM interface and Local Bus.
SDRAM_DATA[8]	B8	I/O	K	Data bit 8 for SDRAM interface and Local Bus.
SDRAM_DATA[9]	B7	I/O	K	Data bit 9 for SDRAM interface and Local Bus.
SDRAM_DATA[10]	A5	I/O	K	Data bit 10 for SDRAM interface and Local Bus.
SDRAM_DATA[11]	D7	I/O	K	Data bit 11 for SDRAM interface and Local Bus.
SDRAM_DATA[12]	B5	I/O	K	Data bit 12 for SDRAM interface and Local Bus.
SDRAM_DATA[13]	A4	I/O	K	Data bit 13 for SDRAM interface and Local Bus.
SDRAM_DATA[14]	C5	I/O	K	Data bit 14 for SDRAM interface and Local Bus.
SDRAM_DATA[15]	B4	I/O	K	Data bit 15 for SDRAM interface and Local Bus.
SDRAM_DATA[16]	A8	I/O	K	Data bit 16 for SDRAM interface and Local Bus.
SDRAM_DATA[17]	C9	I/O	K	Data bit 17 for SDRAM interface and Local Bus.
SDRAM_DATA[18]	A9	I/O	K	Data bit 18 for SDRAM interface and Local Bus.
SDRAM_DATA[19]	B11	I/O	K	Data bit 19 for SDRAM interface and Local Bus.
SDRAM_DATA[20]	A11	I/O	K	Data bit 20 for SDRAM interface and Local Bus.
SDRAM_DATA[21]	D12	I/O	K	Data bit 21 for SDRAM interface and Local Bus.
SDRAM_DATA[22]	B12	I/O	K	Data bit 22 for SDRAM interface and Local Bus.
SDRAM_DATA[23]	C13	I/O	K	Data bit 23 for SDRAM interface and Local Bus.
SDRAM_DATA[24]	A13	I/O	K	Data bit 24 for SDRAM interface and Local Bus.
SDRAM_DATA[25]	C11	I/O	K	Data bit 25 for SDRAM interface and Local Bus.
SDRAM_DATA[26]	B13	I/O	K	Data bit 26 for SDRAM interface and Local Bus.
SDRAM_DATA[27]	A12	I/O	K	Data bit 27 for SDRAM interface and Local Bus.
SDRAM_DATA[28]	C12	I/O	K	Data bit 28 for SDRAM interface and Local Bus.
SDRAM_DATA[29]	B10	I/O	K	Data bit 29 for SDRAM interface and Local Bus.
SDRAM_DATA[30]	A10	I/O	K	Data bit 30 for SDRAM interface and Local Bus.
SDRAM_DATA[31]	D9	I/O	K	Data bit 31 for SDRAM interface and Local Bus.
SDRAM_DQM_N[0]	D10	O	B	Memory Byte enable signal 0 – DQM for SDRAM
SDRAM_DQM_N[1]	C10	O	B	Memory Byte enable signal 1 – DQM for SDRAM
SDRAM_DQM_N[2]	D14	O	B	Memory Byte enable signal 2 – DQM for SDRAM
SDRAM_DQM_N[3]	C15	O	B	Memory Byte enable signal 3 – DQM for SDRAM
SDRAM_RAS_N	C14	O	B	RAS for SDRAM interface
SDRAM_WE_N	B14	O	B	Write Enable for SDRAM Interface

Table. PCI/CARDBUS Interface

PCI/CARDBUS Interface				
Pin Name	Location	I/O/P	Type	Description
PCI_AD[0]	U18	I/O	G	PCI Address/Data bit 0
PCI_AD[1]	U19	I/O	G	PCI Address/Data bit 1
PCI_AD[2]	V19	I/O	G	PCI Address/Data bit 2
PCI_AD[3]	W20	I/O	G	PCI Address/Data bit 3
PCI_AD[4]	W19	I/O	G	PCI Address/Data bit 4
PCI_AD[5]	V18	I/O	G	PCI Address/Data bit 5
PCI_AD[6]	Y19	I/O	G	PCI Address/Data bit 6
PCI_AD[7]	W18	I/O	G	PCI Address/Data bit 7
PCI_AD[8]	V17	I/O	G	PCI Address/Data bit 8
PCI_AD[9]	U16	I/O	G	PCI Address/Data bit 9
PCI_AD[10]	W17	I/O	G	PCI Address/Data bit 10
PCI_AD[11]	V16	I/O	G	PCI Address/Data bit 11
PCI_AD[12]	Y17	I/O	G	PCI Address/Data bit 12
PCI_AD[13]	W16	I/O	G	PCI Address/Data bit 13
PCI_AD[14]	V15	I/O	G	PCI Address/Data bit 14
PCI_AD[15]	Y16	I/O	G	PCI Address/Data bit 15
PCI_AD[16]	V11	I/O	G	PCI Address/Data bit 16
PCI_AD[17]	W11	I/O	G	PCI Address/Data bit 17
PCI_AD[18]	Y11	I/O	G	PCI Address/Data bit 18
PCI_AD[19]	V10	I/O	G	PCI Address/Data bit 19
PCI_AD[20]	W10	I/O	G	PCI Address/Data bit 20
PCI_AD[21]	Y9	I/O	G	PCI Address/Data bit 21
PCI_AD[22]	W9	I/O	G	PCI Address/Data bit 22
PCI_AD[23]	V9	I/O	G	PCI Address/Data bit 23
PCI_AD[24]	Y8	I/O	G	PCI Address/Data bit 24
PCI_AD[25]	W8	I/O	G	PCI Address/Data bit 25
PCI_AD[26]	Y7	I/O	G	PCI Address/Data bit 26
PCI_AD[27]	W7	I/O	G	PCI Address/Data bit 27
PCI_AD[28]	Y6	I/O	G	PCI Address/Data bit 28
PCI_AD[29]	W6	I/O	G	PCI Address/Data bit 29
PCI_AD[30]	U7	I/O	G	PCI Address/Data bit 30
PCI_AD[31]	V6	I/O	G	PCI Address/Data bit 31
PCI_CBE_N[0]	Y18	I/O	G	Command/byte enable bit 0
PCI_CBE_N[1]	W15	I/O	G	Command/byte enable bit 1
PCI_CBE_N[2]	U11	I/O	G	Command/byte enable bit 2
PCI_CBE_N[3]	Y5	I/O	G	Command/byte enable bit 3
PCI_CLK	Y3	I	L	PCI clock
PCI_DEVSEL_N	W13	I	G	PCI Device Select
PCI_FRAME_N	Y12	I	G	FRAME_N is asserted to indicate the start and duration of a transaction. It is de-asserted on the final data phase.
PCI_GNT_N	V7	I	L	PCI Grant
PCI_IDSEL_N	U9	I	L	PCI configuration block ID select
PCI_INTA_N	W5	O	G	PCI interrupt A
PCI_IRDY_N	W12	I/O	G	Initiator read is driven by the master to indicate valid data on a write transaction, or that it is ready to receive data on a read transaction.
PCI_LOCK_N	W14	I/O	L	PCI Lock

PCI/CARDBUS Interface				
Pin Name	Location	I/O/P	Type	Description
PCI PAR	V14	I/O	G	PCI Parity signal
PCI PERR_N	Y14	I/O	G	PCI Parity error signal
PCI REQ_N	V5	I/O	G	PCI Request
PCI RST_N	Y4	I	L	PCI Reset
PCI SERR_N	V13	I/O	G	PCI error signal
PCI STOP_N	Y15	I/O	G	PCI Stop
PCI TRDY_N	Y13	I/O	G	PCI target ready

Table. Power Pin List

Power Pin List				
Pin Name	Location	I/O/P	Type	Description
AGND DIGA	G4	P	N	Analog Ground
AGND DIGA	G3	P	T	Analog Ground
AGND DIGB	K1	P	O	Analog Ground
AGND DIGC	P1	P	O	Analog Ground
AGND PLLG	M1	P	T	Analog Ground
AGND REFA	F3	P	N	Analog Ground
AGND REFB	K3	P	N	Analog Ground
AGND REFC	P2	P	N	Analog Ground
AGND RXA	D2	P	T	Analog Ground
AGND TXA	D1	P	T	Analog Ground
AGND TXB	H2	P	T	Analog Ground
AGND TXG	J2	P	T	Analog Ground
AVCC PHYA	C2	P	P	Analog Vcc
AVCC PLLG	L4	P	P	Analog Vcc
AVCC RXA	D3	P	P	Analog Vcc
AVCC TXA	C1	P	P	Analog Vcc
AVCC TXG	M2	P	P	Analog Vcc
CPU PLL_GND	K18	P	Q	Ground for CPU PLL
CPU PLL_VDD	K17	P	G	Vcc for CPU PLL
Ground	A1	P	NA	Ground for VCC and VCC CORE
Ground	D4	P	NA	Ground for VCC and VCC CORE
Ground	D8	P	NA	Ground for VCC and VCC CORE
Ground	D13	P	NA	Ground for VCC and VCC CORE
Ground	D17	P	NA	Ground for VCC and VCC CORE
Ground	H4	P	NA	Ground for VCC and VCC CORE
Ground	H17	P	NA	Ground for VCC and VCC CORE
Ground	N4	P	NA	Ground for VCC and VCC CORE
Ground	N17	P	NA	Ground for VCC and VCC CORE
Ground	U4	P	NA	Ground for VCC and VCC CORE
Ground	U8	P	NA	Ground for VCC and VCC CORE
Ground	U13	P	NA	Ground for VCC and VCC CORE
Ground	U17	P	NA	Ground for VCC and VCC CORE
SYS_PLL_GND	V12	P	B	Ground for System PLL
SYS_PLL_VDD	U12	P	B	Vcc for System PLL
Thermal Ground	J9	P	NA	Thermal Conductive Ball (Ground)

Power Pin List				
Pin Name	Location	I/O/P	Type	Description
Thermal Ground	J10	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	J11	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	J12	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	K9	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	K10	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	K11	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	K12	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	L9	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	L10	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	L11	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	L12	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	M9	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	M10	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	M11	P	NA	Thermal Conductive Ball (Ground)
Thermal Ground	M12	P	NA	Thermal Conductive Ball (Ground)
VCC	D6	P	NA	3.3 Volt I/O Power Ball
VCC	D11	P	NA	3.3 Volt I/O Power Ball
VCC	D15	P	NA	3.3 Volt I/O Power Ball
VCC	F4	P	NA	3.3 Volt I/O Power Ball
VCC	F17	P	NA	3.3 Volt I/O Power Ball
VCC	K4	P	NA	3.3 Volt I/O Power Ball
VCC	L17	P	NA	3.3 Volt I/O Power Ball
VCC	R4	P	NA	3.3 Volt I/O Power Ball
VCC	R17	P	NA	3.3 Volt I/O Power Ball
VCC	U6	P	NA	3.3 Volt I/O Power Ball
VCC	U10	P	NA	3.3 Volt I/O Power Ball
VCC	U15	P	NA	3.3 Volt I/O Power Ball
VCC_CORE	E3	P	S	Core Vcc
VCC_CORE	L3	P	S	Core Vcc
VCC_CORE	V2	P	S	Core Vcc
VCC_CORE	V8	P	S	Core Vcc
VCC_CORE	Y10	P	S	Core Vcc
VCC_CORE	U14	P	S	Core Vcc
VCC_CORE	P18	P	S	Core Vcc
VCC_CORE	M20	P	S	Core Vcc
VCC_CORE	F20	P	S	Core Vcc
VCC_CORE	B19	P	S	Core Vcc
VCC_CORE	A19	P	S	Core Vcc
VCC_CORE	A15	P	S	Core Vcc
VCC_CORE	B9	P	S	Core Vcc
VCC_CORE	A7	P	S	Core Vcc

Table. Configuration Pin List

Configuration Pin List				
Pin Name	Location	I/O/P	Type	Description
CONFIG_EN	U1	I	L	Enable alternate configuration
CONFIG_MOD[0]	T3	I	L	Configuration Mode bit 0
CONFIG_MOD[1]	U2	I	L	Configuration Mode bit 1
CONFIG_MOD[2]	V1	I	L	Configuration Mode bit 2

Table. No Connect Pin List

No Connect Pin List				
Pin Name	Location	I/O/P	Type	Description
NC	C3	NA	NA	No Connect
NC	A20	NA	NA	No Connect
NC	Y20	NA	NA	No Connect

Mechanical Specifications

The device is packaged in a 256 ball plus 16 PBGA for a total of 272 balls. The package is plastic with an area of 27x27mm and a ball-pitch of 1.27mm. See Package Drawing below.

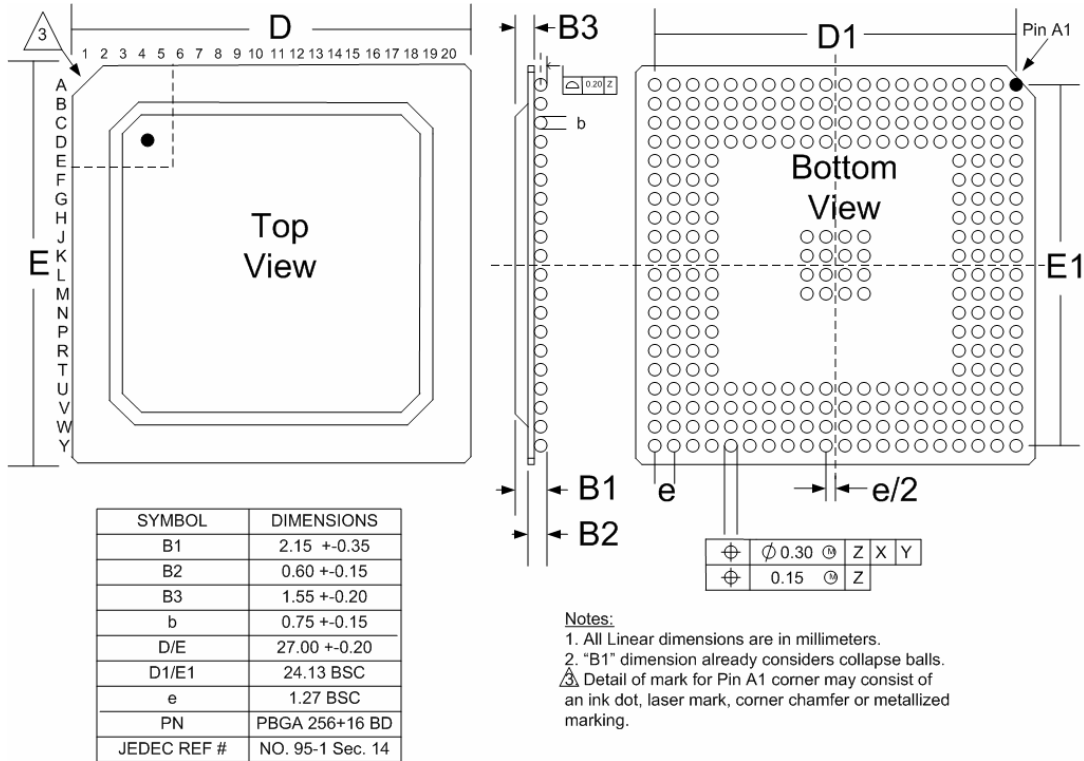


Figure 1 - Package Drawing



- Notes:**
1. All graphics and text are either laser-marked or white ink on black background.
 2. The part number is marked as "MCS1000". The letters following the part number are the temperature range and package type.
 3. Date of manufacture is marked by "YYWW". Where "YY" is two digit year and "WW" is two digit week.
 4. COO is country of origin and may be more than three characters.

Figure 2 - Package Marking