



Features

- Low-power CMOS design
- Powered from USB port
- Single 12 Mhz crystal
- IrDA data rates from 2.4 Kbps to 115.2 kbps in SIR mode
- Support MIR (Medium IR) at 1.152 Mbps
- Support FIR (Fast IR) mode with data rate of 4 Mbps
- Uses standard IrDA transceivers
- USB specification 1.1 compliant.
- Supports all USB standard commands.
- LED driver capable of 650 ma @ 5V, 25% duty cycle
- Full compliance to IrDA 1.4
- Low-profile 28-Pin SSOP package

Applications

- Add-on IrDA dongle
- Cell Phones
- Embedded applications

Application Note

- AN7780

Evaluation Board

- MCS7780-EVB

General Description

The MosChip MCS7780 is a low cost, low power, USB/IrDA Bridge Controller integrated circuit for enabling IrDA wireless data communications through a standard PC USB port. The MCS7780 directly interfaces to both single path and dual path receive IrDA transceiver module architectures and contains a USB controller, IrDA controller, interface logic, and memory buffer for full IrDA 1.4, Support data rate of 2.4 Kbps to 4 Mbps.

MosChip Semiconductor provides Windows 2000/XP™ NDIS/USB driver for enabling the implementation of a cost effective USB/IrDA Adapter solution for wireless data communications.

Commercial Grade

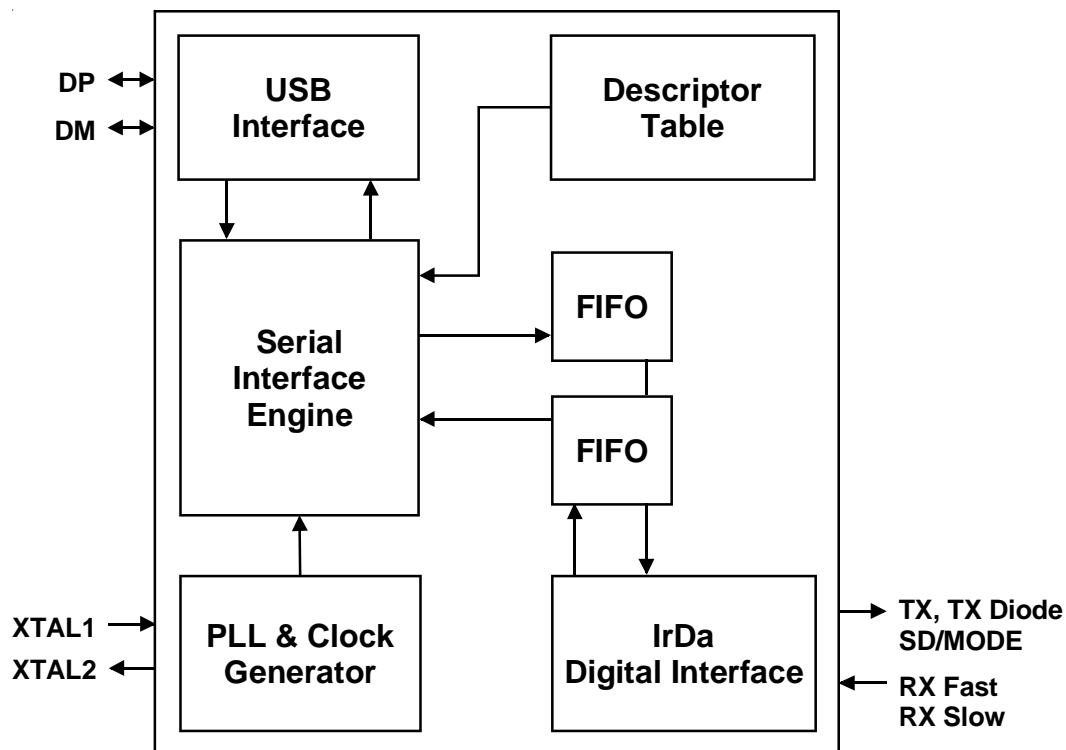
MCS7780CS	28-SSOP	0° C to +70° C
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MCS7780

USB 1.1 to IrDA

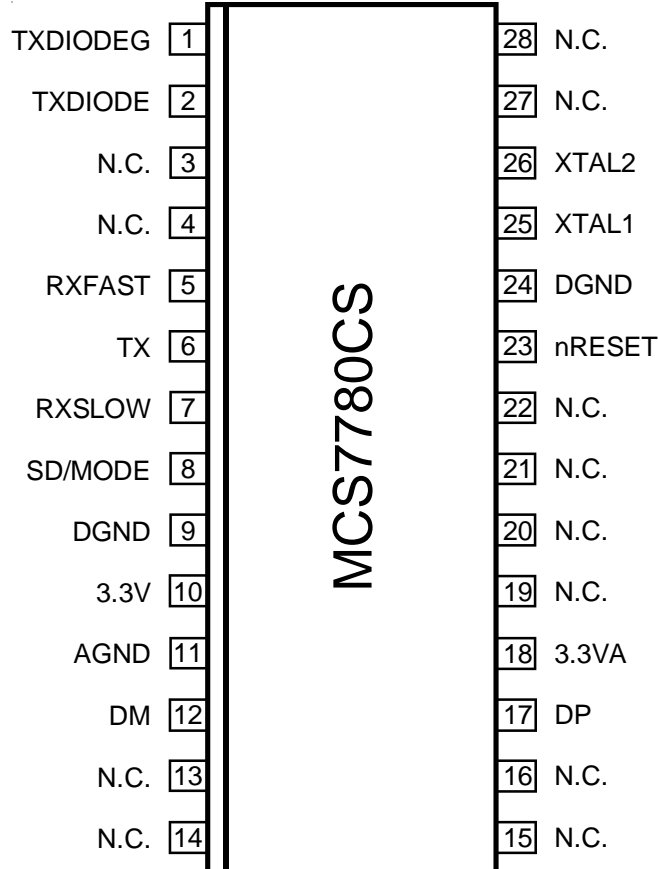


MCS7780 Block Diagram





28-Pin SSOP Package



MCS7780

USB 1.1 to IrDA



Pin Name	Pin	Type	Description
TXDIODEG	1	PWR	Optional LED driver output GND
TXDIODE	2	O	Optional Transmit LED drive output
RXFAST	5	I	Receive data from IR module (Fast)
TX	6	O	Transmit Data output to IR module
RXSLOW	7	I	Receive data from IR module (Slow)
SD/MODE	8	O	Mode control to IR module
DM	12	I/O	USB interface negative data
DP	17	I/O	USB interface positive data
nRESET	23	I	Master Reset, active low
XTAL1	25	I	12 Mhz crystal/clock input
XTAL2	26	O	12 Mhz crystal/clock output
3.3VA	18	PWR	USB transceiver power supply, 5V
3.3V	10	PWR	USB transceiver power supply, 5V
AGND	11	PWR	USB transceiver power supply ground
DGND	9, 24	PWR	Digital Power supply ground



Functional Description

The MCS7780 consists of two major functional blocks, the USB controller and the digital IR transceiver. The USB controller provides a Control, Bulk-In, and Bulk-Out endpoints to the USB host. The digital IR transceiver consists of a transmit and receive interface that connects to an analog IR front end.

This USB/IrDA Bridge Controller has full interface capability to connect between a USB bus, and an IrDA compatible infrared transceiver device.

USB Interface

The USB Device Controller implements USB protocol engine. It has one configuration with a single interface. Two Bulk end-points, with maximum packet size of 64

bytes, are used for data transfers. The MCS7780 uses vendor specific implementation of IR configuration and control. Two vendor specific requests are defined for this purpose, 1. Write Word, and 2. Read Word. The vendor specific requests are piped through control endpoint.

“Write Word” is a 2 phase transaction which can be used to write a single 16-bit register. The setup phase of command supplies both the index and data value to be written into the register. There is no data phase in this transfer.

“Read Word” request is used to read the register contents of MCS7780. It allows reading of one 16-bit register. The setup phase specifies the register address to be read and the data is returned in data phase.

Vendor Specific Device Requests

Write Word

Offset	Field	Size	Value (hex)	Description
0	bmRequestType	1	0X40	Host to device, vendor type, device recipient
1	Brequest	1	0X0E	rite multiple registers
2	Wvalue	2	0XDDDD	Holds the data to be written into the register
4	Windex	2	0X000 - 0X0007	Address of the register to write
6	Wlength	2	0X000	Indicates a two phase transaction

Read Word

Offset	Field	Size	Value (hex)	Description
0	bmRequestType	1	0XC0	Device to host, vendor specific
1	BRequest	1	0X0F	Read registers
2	Wvalue	2	0x0000	Not used
4	Windex	2	0X0000 - 0X0007	Address of register to read
6	Wlength	2	0X0001	Allows only one registers to read

MCS7780

USB 1.1 to IrDA



Digital IR Transceiver

The Digital IR Transceiver is responsible for driving the transmit diode and receiving the digital input from an analog IR front end. The primary components are the transmit modulator, the receive demodulator, the FIFO, the analog transmit section, and the register array.

By programming the registers in the register array, the device's operation is determined. Various registers are used to specify operations such as the modulation scheme, the baud rate, the current frame size in the FIFO, the RX input selection, etc.

In steady state transmit operation, the USB controller is filling the FIFO with data while the Digital IR Transceiver is emptying it via the transmit modulator. In steady state receive operation, the USB controller is emptying the FIFO while the RX demodulator is filling the FIFO.

IR FRAMING

Framing involves adding wrappers around payload received from NDIS to make a valid IR frame. MCS7780 uses a custom framing style to achieve low gate count. The hardware and software together play a role in making of SIR, MIR, and FIR frames.

Mode Register: offset 0X00

Name	Bit	Access	Default	Description
FIR	0	R/W	0	1 = Puts the device in fast infrared mode (4MHz). 0 = When cleared, puts the device in SIR/MIR mode based on Baud Rate register. IR needs be reset when this bit is changed.
SIR	1	R/W	0	1 = The SIR pulse width of 1.6 us is used. 0 = The SIR pulse used is 3/16th of bit time. IR needs be reset when this bit is changed.
BBTG	2	R/W	1	1 = Enables back to back transmission with no inter packet gap. Invalid in SIR mode.
ASK	3	R/W	0	1 = Puts the device in ASK mode. 0 = Device not in ASK mode. IR needs be reset when this bit is changed.
PARITY	4	R/W	0	1 = Odd parity to be used by ASK. 0 = Even parity is used IR needs be reset when this bit is changed.
RATE	[7:5]	R/W	0X1	Baud rate selector. IR needs be reset when this bit is changed.

PLLPWD	8	R/W	1	1 = To enable power down feature of the PLL 0 = power down feature of the PLL disabled.
DRIVER	9	R/W	0	1 = Upon initialization. 0 = Upon reset.
DTD	10	R/W	1	1 = Device determines the transfer direction automatically. 0 = The direction is controlled by software by writing a 1 (TX) or 0 (RX) in DIR bit of this register
DIR	11	R/W	0	This bit controls the direction of transfer. 1 = Transmit 0 = Receive This bit is valid only when AUTO = 0. The software should check the CHGDIR bit before writing to this bit.
SIPEN	12	R/W	1	1= Enables the automatic generation of SIP pulse from the hardware. 0 = Disables the auto SIP generation. Need be generated by software through vendor specific commands.
SENDSIP	13	R/W	0	On detecting a transition from low to high on this bit, the device generates a SIP.
CHGDIR	14	R	1	1 = Software is allowed to change the transfer direction by writing to DIR bit. 0 = Direction change is not allowed. Software shall poll until it goes high before changing the direction.
RESET	15	R/W	1	0 = Resets the bridge and IR TOP modules. This bit self clearing.

MCS7780

USB 1.1 to IrDA



Baud Rate	Frequency selected
0	2.4 kbps
1	9.6 kbps
2	19.2 kbps
3	38.4 kbps
4	57.6 kbps
5	115.2 kbps
6	0.576 Mbps
7	1.152 Mbps

Framing Register: offset 0X01

Name	Bit	Access	Default	Description
STAL	[7:0]	R/W	0X0	LSB 6 bits indicate the number of STAs to be used Bit-7 = 1, The 6 LSBs are used as number of STAs to be used. Bit-7 = 0, Uses the values hard coded in the design. IR needs be reset when this bit is changed.
IPG	[15:8]	R/W	0X0	Inter packet gap specified in terms of number of bit times (MIR) or chip time (FIR). IR needs be reset when this bit is changed. Bit-15 = 1, The 6 LSBs are used the inter packet gap to be used. Bit-15 = 0, Uses the values hard coded in the design. IR needs be reset when this bit is changed.



XCVR Register: offset 0X02

Name	Bit	Access	Default	Description
MODE0	0	R/W	0	To configure the transceiver. The usage varies with the transceiver make and is reflected in the transceiver truth table.
STFIR	1	R/W	0	To configure the transceiver. The usage varies with the transceiver make and is reflected in the transceiver truth table.
XCVR	2	R/W	0	1 = Puts the transceiver in configuration mode. 0 = Puts the transceiver in data transfer mode.
RXFAST	3	R/W	0	1 = Causes the device to use RXFAST as the input pin for receive from transceiver. 0 = Causes the device to use RXSLOW as the receive signal.
TXCUR	[6:4]	R/W	0	Sets the current control bits of the pad that drives TX-LED. This controls the current supplied to TX-LED.
MODE1	7	R/W	0	To configure the transceiver. The usage varies with the transceiver make and is reflected in the transceiver truth table.
SMODE0	8	R/W	1	Value of MODE0 to be configured to put it into shut down. Varies with transceiver make.
SMODE1	9	R/W	0	Value of MODE1 to be configured to put it. in shut down. Varies with transceiver make.
INVTX	10	R/W	0	1 = inverts the data bits being fed into transceiver for transmit. 0 = the transmit line works as active high signal.
INVRX	11	R/W		1 = RXD line from transceiver is treated as an active low signal 0 = RXD line from transceiver is treated as an active high signal.
EEDATA	[15:12]	R	0	Loaded from the EEPROM.

MCS7780

USB 1.1 to IrDA



The table below shows the usage of XCVR Register for various Transceivers.

Vendor	Code	Dynamic Configuration			
		MODE0	MODE1	STC_FIR	Latched From
Vishay TDFU6614	0	1->0	0	0	TXD
Vishay TDFU6102	0	1->0	0	0	TXD
SHARP GP2W100YP	1	1->0	0	1	TXD
Agilent 3602/3600	2	Can switch pins dynamically. There is no latching mechanism			

SIP Resister: offset 0X03

Name	Bit	Access	Default	Description
SIPON	[6:0]	R/W	0X4C	Specifies pulse width of the SIP in terms of number of 48 MHz clocks.
SIPOFF	[15:7]	R/W	0X154	The SIP low time specified as of number of 48MHz clocks.

MINRXPW Register: offset 0X04

Name	Bit	Acess	Default	Description
MNRXW	[15:0]	R/W	0X00	Minimum pulse width of the signal to be received. 0 = device uses the hard coded values. X = non zero device uses the value specified from this register.



TXPW Register: offset 0X05

Name	Bit	Access	Default	Description
TXPW	[15:0]	R/W	0X00	Pulse width of the signal transmitted. 0 = device uses the hard coded values X = non zero value, device uses the value specified from this register.

RFIFO2: offset 0X06

Name	Bit	Access	Default	Description
TIMEOT	[7:0]	R/W	0X0A	Timeout specified in terms of 50ms. Used in SIR mode to abort a receive if idle for long period specified by this register. N => N*50 ms timeout.
TRSHD	[14:8]	R/W	0X40	FIFO Threshold
CLRFF	15	R/W	0	1 = Clear FIFO pointers 0 = FIFO pointers not cleared This bit is self clearing

RESV: offset 0X07

Name	Bit	Access	Default	Description
RESV	[15:2]	R/W	0X0A	Reserved
IRINRX	1	R	0	1 = Indicates that the receive is in progress 0 = Indicates that receive is not in progress
IRINTX	0	R	0	1 = Indicates that the transmit is in progress 0 = Indicates that transmit is not in progress

MCS7780

USB 1.1 to IrDA



Absolute Maximum Ratings

Supply Range	3.8 Volts
Voltage at any pin	GND – 0.3 to VCC +0.3
Operating Temperature	-45° C to 90° C
Storage Temperature	-65° C to 150° C
Package Dissipation	500 mW
ESD	±2000 Volts
Latch up	220 mA

DC Electrical Specification

T = 0° C to 70° C, VCC = 3.3V ± 10% unless otherwise specified.

Symbol	Parameter	3.3V		Unit	Condition
		Min	Max		
VCC		3.0	3.6	V	
Viclck	Clock input low level clock	-0.5	0.6	V	External
Vihck	Clock input high level clock	2.4	VCC	V	External
Vil	Input low level		1.08	V	CMOS
Vih	Input high level	2.1		V	CMOS
Vol	Output low level		0.4	V	I _{ol} = 4 mA
Voh	Output high level	1.85		V	I _{oh} = 4 mA
Iil	Input leakage current	-10	+10	µA	
Icc	Operating current	12	19	mA	
Cp	Input pin Capacitance		5	pF	



AC Electrical Specification

T = 0° C to 70° C, VCC = 3.3V ± 10% unless otherwise specified.

Symbol	Parameter	3.3V		Unit	Condition
		Min	Max		
CLKA	USB clock frequency	6	12 48	MHz	+/- 50PPM

Revision Notes

Date

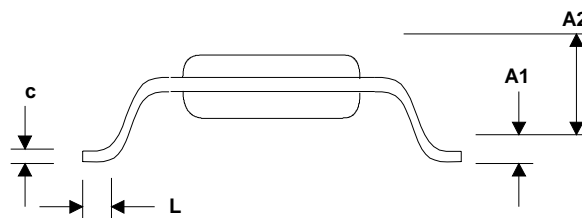
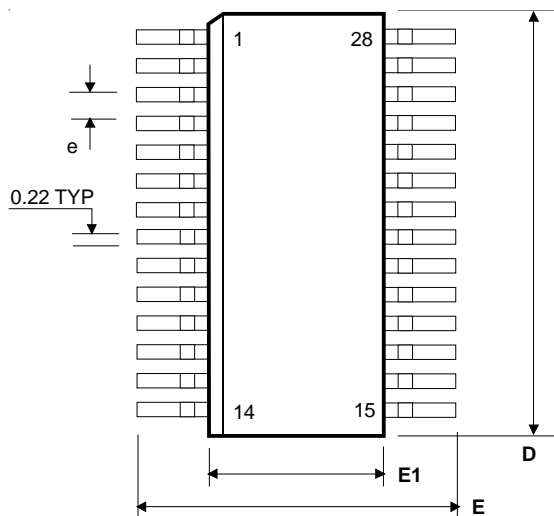
1.0	Corrections	02/04
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MCS7780

USB 1.1 to IrDA



28-Pin SSOP Package



SYMBOL	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A1	0.05	0.21	0.020	0.08
A2	1.65	1.80	0.650	0.708
e	0.65 TYP		0.026 TYP	
D	10.00	10.4	3.93	4.09
E1	5.2	5.4	2.05	2.12